REMARKS

Claims 1-12, 17 and 18 are pending in this application. By this Amendment, claims 1, 3-5, 11 and 12 are amended. Support for the amendments to claims 1, 3-5, 11 and 12 can be found at, for example, in Figs. 4, 5 and 7. Specifically, the added features in claims 3 and 11 can be found, for example, in Fig. 4; and the added feature in claims 4 and 12 can be found, for example, in Fig. 7. No new matter is added. Claims 13-16 are canceled without prejudice to, or disclaimer of, the subject matter recited in these claims. Reconsideration of the application in view of the foregoing amendments and the following remarks is respectfully requested.

The Office Action rejects claims 1, 3, 5, 11, 17 and 18 under 35 U.S.C. §103(a) over U.S. Patent No. 6,756,252 to Nakanishi in view of U.S. Patent No. 6,445,069 to Ling et al. (Ling); rejects claims 6, 7, 12, and 13 under 35 U.S.C. §103(a) over Nakanishi with Ling and further in view of U.S. Patent No. 6,625,032 to Ito et al. (Ito); and rejects claims 2, 4, 8-10 and 14-16 over Nakanishi with Ling or Nakanishi with Ling and Ito and further in view of JP-A-01-164044 (JP '044). The rejection of claims 13-16 is moot in view of the cancellation of claims 13-16. These rejections are respectfully traversed with respect to claims 1-12, 17 and 18.

Claim 1 recites, among other features, an insulating section formed adjacent to the chip component, the insulating section having an inclined surface descending in an outward direction from the chip component, the inclined surface being a convex surface that draws a curve on a view from which a cross section perpendicular to the first surface of the chip component is taken.

Claim 5 recites, among other features, a step of forming an insulating section adjacent to the chip component to have an inclined surface descending in an outward direction from

the chip component, the inclined surface being a convex surface that draws a curve on a view from which a cross section perpendicular to the first surface of the chip component is taken.

None of the applied references taken alone, or in combination, teach, or reasonably would have suggested these features.

Nakanishi teaches a method for creating electrical interconnects between a semiconductor die 10 and a package substrate 84. However, Nakanishi does not teach nor cannot reasonably be considered to have suggested, the inclined surface being a convex surface with all of the configurations of features positively recited in claims 1 and 5. Nakanishi teaches in general as shown for example in Fig. 10A, 10B, 11 and 15, that its insulating layer 104 merely extends from the upper surface of die 10 at a downward slope. Figs. 13, 14A, 14B in Nakanishi appear to disclose that the insulating layer 104a, 104b applied over substrate contacts 100 is raised to bulge slightly outward. Nevertheless, at least Figs. 13, 14A and 14B cannot be relied upon to disclose, or reasonably to have suggested the subject matter of claims 1 and 5 because these claims recite that the inclined surface is a convex surface that draws a curve on a view which is taken from a cross section perpendicular to the first surface of the chip component. The insulating layer 104a, 104b located above substrate contacts 100 is not positioned at a location that is at a cross section perpendicular to the upper surface of die 10.

Furthermore, with respect to combining the prior art references, Ling is relied upon for allegedly teaching a pad formed on a first surface and a metal layer formed of a plurality of layers; Ito is merely relied upon for allegedly teaching a dispersant ejecting method; and JP '044 merely discloses electrode land portions formed of a single layer of Al or Au. Thus, these prior art references do not overcome the above-referenced shortfall in the application of Nakanishi with respect to the features recited in claims 1 and 5.

In view of the above, Nakanishi, Ling, Ito, and JP '044, taken alone or in any permissible combination, do not teach, nor would they reasonably have suggested, the combinations of all of the features positively recited in claims 1 and 5. Further, claims 2-4, 6-12, 17 and 18 also would not have been suggested by the applied prior art references for at least their respective dependence directly or indirectly on allowable base claims, as well as for the separately patentable matter that each of these claims recite. Accordingly, reconsideration and withdrawal of the rejections of the pending claims over any permissible combination of the applied prior art references are respectfully requested.

Claims 1-18 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting over claims 1-34 of co-pending U.S. Patent Application No. 10/788,449 in view of Nakanishi and Ling. The rejection of claims 13-16 is moot in view of the cancellation of claims 13-16. This rejection is respectfully traversed with respect to claims 1-12, 17 and 18.

U.S. Patent Application No. 10/788,449, Nakanishi and Ling each fail to teach or suggest an insulating section formed adjacent to the chip component, the insulating section having an inclined surface descending in an outward direction from the chip component, the inclined surface being a convex surface that draws a curve on a view from which a cross section perpendicular to the first surface of the chip component is taken, as recited in claims 1 and 5 and as discussed above.

For the foregoing reasons, claims 1 and 5, as well as the claims depending therefrom, are not rendered obvious by claims 1-34 of U.S. Patent Application No. 10/788,449 in view of Nakanishi and Ling.

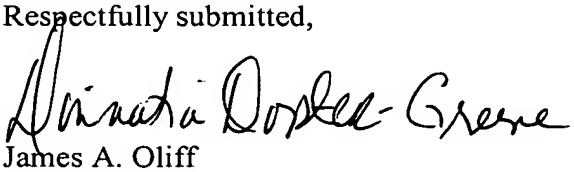
Accordingly, reconsideration and withdrawal of the rejection on the ground of the non-statutory obviousness-type double patenting rejection are respectfully requested.

Alternatively, we believe that MPEP §822.01 provides guidance that if the "provisional" double patenting rejection in one application is the only rejection remaining in that application, which is the case here based on the claim amendments and arguments presented above, the Examiner should then withdraw that rejection and permit the application to issue as a patent thereby converting any "provisional" double patenting rejections in other applications into double patenting rejections at the time the one application issues as a patent.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-12, 17 and 18 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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